AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph that begins on application page 11, line 2, and ends on application page 11, line 4, with the following replacement paragraph:

FIG. 2 is a diagram showing waveforms of an output signal 131 of a filter 106, an output signal 132 of a loop filter 103 and an output signal 133 of an adder 102~~133~~.

Please replace the paragraph that begins on application page 11, line 5, and ends on application page 11, line 7, with the following replacement paragraph:

FIG. 3 is a diagram showing waveforms of the output signal 131 of the filter 106, the output signal 132 of the loop filter 103 and the output signal 133 of the adder 102~~133~~.

Please replace the paragraph that begins on application page 11, line 9, and ends on application page 11, line 11, with the following replacement paragraph:

FIG. 5 is a diagram showing waveforms of the output signal 131 of the filter 106, the output signal 132 of the loop filter 103 and the output signal 133 of the adder 102~~133~~.

Please replace the paragraph that begins on application page 15, line 20, and ends on application page 15, line 24, with the following replacement paragraph:

Next, an example of the timing error detecting/correcting method will be described. FIGS. 2 and 3 are diagrams showing the

waveforms of an output signal 131 of the filter 106, an output signal 132 of the loop filter 103 and an output signal 133 of the adder 102~~133~~.

Please replace the paragraph that begins on application page 16, line 13, and ends on application page 17, line 5, with the following replacement paragraph:

However, when the output signal 131 and the output signal 132 are displaced from each other in timing due to dispersion of the loop filter 103 or the like, the output signal 133 of the adder exhibits the characteristic of a sine wave as shown in FIG. 3[[2]]. The amplitude of the output signal 133 is more greatly increased as the timing error between the output signal 131 and the output signal 132 is larger. Accordingly, by detecting the output signal 133 of the adder 102, the timing error between the output signal 131 and the output signal 132 can be detected. The A/D converter 108 converts this output signal 133 to a digital signal, and the delay controller 110 calculate amplitude information from the digital signal output from the A/D converter 108 and outputs a control signal to the delay circuit 111 and the delay circuit 112 on the basis of the above calculation result. The delay controller 110 generates this control signal so that the amplitude of the output signal

133 of the adder 102 is reduced, whereby the timing error in the two-point modulation can be corrected.

Please replace the paragraph that begins on application page 18, line 8, and ends on application page 18, line 22, with the following replacement paragraph:

The phase modulation data input at the timing error detection time is not limited to the sine wave, and any waveform may be used. It is more preferable that the phase modulation data is phase modulation data in a narrow band. Furthermore, the delay circuit is provided to both the side at which the modulation is applied to the frequency divider 105 and the side at which the modulation is applied to VCO 101, however, the delay circuit may be provided to only one of them. In this case, the timing at the side at which no delay circuit is provided is fixed, and thus the timing error can be corrected by controlling the timing at the side at which the delay circuit is provided. Furthermore, the inverter 113~~115~~ may be provided to the side at which modulation is applied to VCO 101 in place of the provision thereof to the side at which the modulation is applied to the frequency divider 105.